	Search Text
1	(mak$4 permi$5) same transparen$4 same latch$4 and clock adj (buffer driver)
2	(mak$4 permi$5) same transparen$4 same latch$4 and clock adj (buffer driver) and delay same (latch$4 buffer driver)
3	(mak$4 permi$5) same transparen$4 same latch$4 and clock adj (buffer driver) and delay same (latch$4 buffer driver) and "716"/$.ccls.
4	(mak$4 permi$5) same transparen$4 same latch$4 same timing same (model$4 static anal$7 simul$4 synthes$7) and clock adj (buffer driver) and delay same (latch$4 buffer driver)
5	transparen$4 same latch$4 same timing same (model$4 static anal$7 simul$4 synthes$7) and clock adj (buffer driver) and delay same (latch$4 buffer driver)
6	transparen$4 same latch$4 same timing same (model$4 static anal$7 simul$4 synthes$7) and clock adj (buffer driver) and delay same (latch$4 buffer driver) and delay same latch$4
7	transparen$4 same latch$4 same timing same (model$4 static anal$7 simul$4 synthes$7) and clock adj (buffer driver) and delay same (latch$4 buffer driver) and delay same latch$4 and (user engineer designer) same delay
8	allow$4 same transparent$4 same latch$4
9	clock same (transparen$4) same latch$4 and clock same (nontransparen$4 non adj transparent$4) same lactch$4
10	(transparen$4) same latch$4 and (nontransparen$4 non adj transparent$4) same lactch$4
11	(transparen$4) same latch$4 same clock near4 (delay$4 adjust$5 modif$6)
12	(transparen$4) same latch$4 same clock near4 (delay$4 adjust$5 modif$6) and clock near4 (edge overlap$4 rising falling)
13	(transparen$4) same latch$4 same clock near4 (delay$4 adjust$5 modif$6) and clock near4 (edge overlap$4 rising falling) and "716"/$.ccls.
14	(transparen$4) same latch$4 same clock near4 (delay$4 adjust$5 modif$6) and clock near4 (edge overlap$4 rising falling) and "716"/$.ccls. and @ad<="20030926"
15	(transparen$4) same (nontransparen$4 non adj transparent$4) same lactch$4
16	(transparen$3 nontransparen$3 non adj transparent$3) same lactch$4 clock same (chang$4 modif$6 adjust$5)
17	(transparen$3 nontransparen$3 non adj transparent$3) same lactch$4 clock same (chang$4 modif$6 adjust$5) and "716"/$.ccls. and @ad<="20030926"
18	(transparen$3 nontransparen$3 non adj transparent$3) same lactch$4 clock near5 (chang$4 modif$6 adjust$5) and "716"/$.ccls. and @ad<="20030926"
19	(transparen$3 nontransparen$3 non adj transparent$3) same lactch$4 clock near5 (chang$4 modif$6 adjust$5) and "716"/$.ccls. and @ad<="20030926" and (sta (static tool model) near3 timing)
20	(transparen$3 nontransparen$3 non adj transparent$3) same lactch$4 clock near5 (chang$4 modif$6 adjust$5) and "716"/$.ccls. and @ad<="20030926" and (sta (static tool model) near3 timing) and clock with (overlap$4 delay$5)
21	(transparen$3 nontransparen$3 non adj transparent$3) same lactch$4 same clock near5 (chang$4 modif$6 adjust$5) and "716"/$.ccls. and @ad<="20030926" and (sta (static tool model) near3 timing) and clock with (overlap$4 delay$5)

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22	(transparen$3 nontransparen$3 non adj transparen$3) same latch$4 same clock same (delay$4 chang$4 modif$6 adjust$5) and "716"/$.ccls. and @ad<="20030926"
23	(transparen$3 nontransparen$3 non adj transparen$3) same latch$4 same clock near4 (delay$4 chang$4 modif$6 adjust$5) and "716"/$.ccls. and @ad<="20030926"
24	(transparen$3 nontransparen$3 non adj transparen$3) same latch$4 same clock near4 (alter$5 delay$4 chang$4 modif$6 adjust$5) and "716"/$.ccls. and @ad<="20030926"